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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,602	07/05/2005	Hong-Sick Park	8071-152T	7109

7590 12/16/2008

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11797

EXAMINER	
MULPURI, SAVITRI	
ART UNIT	PAPER NUMBER
2812	

MAIL DATE	DELIVERY MODE
12/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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DETAILED ACTION

This action is in response to the applicant's communication filed on 8/29/2008.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27-35, 40-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chae (US 6,919,931) in combination with Kelly et al (US 6,524,663) or Kodas et al (US 2003/0124259A) and Qian(US 6,365,968) and **Yamanaka et al (**US 6,521,525)

Chae teaches a method of manufacturing and a thin film transistor device for array panel, the method comprising:

Forming a gate wire on an insulating substrate "22", the gate wire including a gate line "13", a gate electrode"26", and a gate pad"41";

With respect to claims 4-9, sequentially depositing agate insulating layer ""51", amorphous silicon layer "53", and ohmic contact layer"55" on the gate wire;

Patterning the ohmic contact layer and the amorphous layer by photolithography;

Forming a data wire on the ohmic contact layer, and the adapt wire including source and drain electrodes "28, 30", a data line "15", data pad (not shown);

forming a protective layer "57"on the data wire, the protective layer having a first contact hole "59" exposing the drain electrode, a second contact hole exposing t he gate pad "61"and a third contact hole exposing the data pad (not shown) and;

forming pixel electrode"17", a subsidiary gate pad or transparent pad electrode "43" on gate pad "41", add subsidiary data pad or transparent pad electrode (not shown) on data pad on the protective layer, the pixel electrode being connected to the drain electrode through first contact hole, the subsidiary gate pad being connected to the gate pad through the second contact hole, the subsidiary data pad being connected to the data pad through the third contact hole (see fig 22,3 4A-5 and related description).

With respect to claim 9 Chae also teaches forming protective layer with prominent and depressed portions

Chae does not teach forming an organometallic layer by coating a photosensitive organometallic complex; placing a photomask over the oragnometallic layer such that a predetermined region of the oragnometallic is exposed; exposing the organometallic layer to the light through a photomask; and developing the organometallic layer.

Kelly et al teaches a method of forming a metal pattern for integrated circuits comprising: forming an organ metallic layer by coating a photosensitive organometallic complex; exposing the organometallic layer to light through a photomask; and forming a metal a pattern by developing the organometallic layer(see abstract and col1, lines 46-54). Kelly further teaches making integrated circuits by forming metallization by using organic metal compounds, wherein metals includes Cu Ni, gold , or any other suitable metals (see col. 8, lines 47-50; col. 9, lines 46-49 It would have been obvious to one of ordinary skill in the art to form metal pattern in the invention of Chae by forming organometallic layer by coating a photosensitive organometallic complex and exposing the organometallic layer to light through photomask and developing and

forming a metal pattern by developing the organometallic layer because such process is electroless plating and gives good quality result and metal pattern can be formed on the insulator or on the semiconductor or on the conductors(see col. 1, lines 35-45).(see fig. 2, -4 and related description).

With respect to claims 34 neither Chae nor Kelly teaches organic material containing silver.

Kodas et al (US 2003/0124259A). teaches metal organic precursor composition containing UV sensitive organic ligand by using organic metallic complex containing silver or aluminum to form metal as a contact on semiconductor materials(see para 0023,para 0049,para0058). Kodas et al also discloses ultraviolet irradiation by using photo mask to form metal pattern (para 0168). It would have been obvious to one of ordinary skill in the art to form silver or Al metal pattern in the invention of modified invention Chae because Kelly gives a choice of using any other suitable metals alternative disclosed materials such Pd, Pt Ag.

Clearly both Kelly and Kodas (para0168) teach, "The development of organometallic layer is made by way of organic solvent".

Kelly teaches organometallic compound is either in liquid sate or solid state to form metal pattern for integrated circuits by coating a photosensitive organometallic complex; exposing the organometallic layer to light through a photomask; and forming a metal a pattern by developing the organometallic layer(see abstract and col1, lines 46-54). Kelly further teaches making integrated circuits by forming metallization by using organic metal compounds, wherein metals includes Cu Ni, gold , or any other

suitable metals (see col. 8, lines 47-50; col. 9, lines 46-49 . Kodas teaches organometallic compound is as organic solvent. It would have been obvious to one of ordinary skill in the art to use organic metallic compound as a liquid or solid state because both forms are suitable to form metal pattern for integrated circuits as taught by Kelly et al or Kodas.

None of the above references teach embossing surface. Qian teaches forming embossing surface on the protection layer "118" by using a photoresist with variable thickness and then followed by oxide metal layer (abstract and col.2, lines 34-47). It would have been obvious to one of ordinary skill the art to form embossing surface in the modified invention invention of Chae because embossing the surface by suing photoresist with variable thickness would give good adhesion between embossed layer and the subsequently deposited layer.

With respect to new limitation in claims 30 and 31, 40-45 none of the above applied refences teach embossing the porptective layer pixel electrode gate pad and data pad are formed directly on the embossed protective layer (Fig. 6 (19) and related description. Yamanaka et al teaches such limitations (fig. 9, and fig250. It would have been obvious to one of ordinary skill in the art to form embossed surface of the photoresist layer and form reflection layer would give optimum reflection characteristics for the display TFT (col.24, lines 48-59).

Response to Arguments

Applicant's arguments filed 8/29/2008 have been fully considered but they are not persuasive. Applicant argues that Kelly fails to teach or suggest a method which includes utilizing an organometallic layer which when developed after being exposed to light through a photomask directly forms a final metal pattern, as recited in the new claim 27 or a method in claim 30 and 31. In contrast Kelly describes a method of forming a metal by using an organometallic compound. However, the direct product made by organometallic is only a surface activation i.e., a seed film for electroless plating. Thus Kelly requires that additional steps, such as electroless plating be performed on the surface activation film before final metal film is formed which can be used for wires, etc, as disclosed in absatrctcol.1, lines 46-55). . Accordingly the surface activation film formed in Kelly is clearly is not a final metal film as required by claim 27 nor the surface activation film of Kelly be used for gate wires, data wires or pixel electrodes As required by claims 30, 31. Rather, in Kelly, final product a final pattern of final metal film used for wires is formed by subsequent step of electroless plating on the surface activation film. However, Kelly uses the same technique as claimed of forming organ metallic layer by coating photosensitive organometallic complex, placing a photomask over the organometallic layer such that a predetermined pattern orgnaometallic layer is exposed, exposing the organometallic layer to light through photomask, and developing the organometallic layer. Though Kelly teaches thin metal film as seed layer Kodas teaches the same technique to form the metal line without

subsequent electroless deposition.(para 0168). Yamanaka et al teaches newly recited limitations as mentioned above.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Savitri Mulpuri whose telephone number is 571-272-1677. The examiner can normally be reached on Mon-Fri from 8 a.m. to 4.30 p.m...

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber, can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Savitri Mulpuri/

Primary Examiner, Art Unit 2812